1. An apparatus providing a specialized microprocessor or hardwired circuitry to process packets for data communications and control comprising:

a) a microprocessor in communication with a memory for data and program storage, the processor configured to process instruction words of a fixed length of bits and to decode not more than four instructions;

b) two general-purpose registers in communication with the microprocessor; and

c) a state machine controlling the operation of the microprocessor, the state machine having four states, a RESET state, a FETCH state, a WAIT state and a JUMP state.

2. The apparatus of claim 1 further including:

a) means to handle internal events coupled to said microprocessor; and

b) means to handle external events coupled to said microprocessor;

3. The apparatus of claim 1 further including a DMA register coupled to said microprocessor.

4. The apparatus of claim 3 further including at least one timer coupled to said microprocessor.

5. The apparatus of claim 1 wherein the packets are Internet protocol packets.

6. The apparatus of claim 2 wherein the means to handle internal events is responsive to events originating from at least one of:

a) timers;

b) real-time timers; or

c) watchdog logic.

7. The apparatus of claim 2 wherein the means to handle external events is responsive to events originating from:

a) the reception of a packet;

b) notification that data is ready to be transmitted; or

c) notification that data has been transmitted.

8. The apparatus of claim 7 wherein the packets contain video information.

9. The apparatus of claim 1 further including a CSUM register and a DMA register coupled to said microprocessor.

10. The apparatus of claim 1 further including a comparitor coupled to both said general-purpose registers to produce an output to the microprocessor representative of the relative data content between the two registers.

11. The apparatus of claim 10 wherein the comparitor output is a pair of flags, namely, an equal flag and a greater than flag.

12. The apparatus of claim 1 further including a CSUM register coupled to the microprocessor over a data path, the CSUM register configured to calculate a one's complement of each instruction word received over the data path.

13. The apparatus of claim 12 that calculates a checksum value that matches a pre-chosen value.

14. The apparatus of claim 1 wherein the MOVE instruction has 14 bits dedicated to define a source address and 14 bits dedicated to define a destination address.

15. An apparatus providing a specialized microprocessor or hardwired circuitry to process packets for data communications and control comprising:

a) a microprocessor in communication with a memory for data and program storage, the processor configured to process instruction words of a fixed length of bits and to decode not more than two instructions consisting of LOAD and MOVE;

b) two general-purpose registers in communication with the microprocessor; and

c) a state machine controlling the operation of the microprocessor, the state machine having four states, a RESET state, a FETCH state, a WAIT state and a JUMP state.

16. The apparatus of claim 15 further including the following means, each coupled to said microprocessor:

a) means to handle internal events;

b) means to handle external events;

c) a DMA register;

d) a CSUM register; and

e) at least one timer.

17. The apparatus of claim 16 wherein the packets are Internet protocol packets.

18. The apparatus of claim 17 wherein the packets contain video information.

19. The apparatus of claim 18 wherein the means to handle external events is responsive to:

a) the reception of a packet;

b) notification that data is ready to be transmitted; or

c) notification that data has been transmitted.

20. An apparatus providing a specialized microprocessor or hardwired circuitry to process packets for data communications and control comprising:

a) a microprocessor in communication with a memory for data and program storage, the processor configured to process instruction words of a fixed length of bits and to decode not more than four instructions;

b) two general-purpose registers in communication with the microprocessor;

c) a state machine controlling the operation of the microprocessor, the state machine having three states, a FETCH state, a WAIT state and a JUMP state;

d) means to handle internal events;

e) means to handle external events;

f) a DMA register;

g) a CSUM register; and

h) at least one timer.